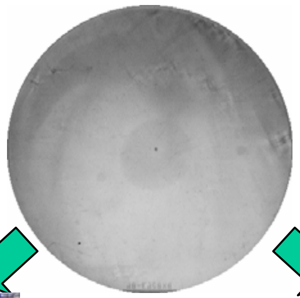
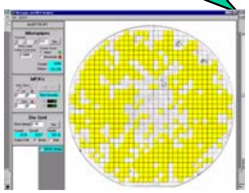
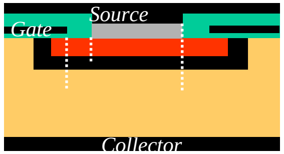
Development of 3" and 4" SiC Substrates, Epitaxy, and MW Class Power Devices

Cree, Inc.



Polarized Light Image of a Recent 3 inch 4H-SiC Wafer





Vertical DMOSFET

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Goals, Objectives and Main Technical Approach

SiC n-type Substrates

- Micropipe densities <0.2 cm^{-2}
- High Purity, high lifetime substrates

SiC Epitaxy

- 3" and 4" Epi, 5% uniformity thickness/doping for 10kV
- Reduce total electrically active defects in epi to <0.5 cm^{-2}

Power Devices

- 10 kV PiN Diodes and 10 kV Power MOSFETs

Key Accomplishments

- Obtained micropipe density of 0.18 cm^{-2} on 3" n-type SiC wafer, and 7 cm^{-2} on 4" SiC wafer
- Achieved epi thickness uniformity of 0.2% for 160 μm thick films, and <5% doping on 100 μm thick films.
- Reduced total electrically active defect density in 160 μm thick epilayers to <0.17 cm^{-2}
- Demonstrated 10 kV, 50 Amp SiC PiN Diodes with V_f = 4.2 V. 60% of these diodes had V_f drift less than 100 mV.
- Demonstrated 10 kV DMOSFETs with $R_{DS(on)}$ of 100 mΩ-cm^2

Major Impact of Technology & Technology Transition Plan

- Substantially increased device yields for high power DoD switching devices
- Enables path to new Ultra-high voltage device applications (>25 kV)
- Enables low cost for commercial entry into high power switching markets
- Resulting SiC devices allow large reduction in size and weight of power supplies for power distribution, traction control, and high pulse power conditioning for military applications